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United States Patent [19]

Harari et al.

[11] Patent Number: 6,149,316

[45] Date of Patent: *Nov. 21, 2000

[54] **FLASH EEPROM SYSTEM**

[75] Inventors: **Eliyahou Harari**, Los Gatos; **Robert D. Norman**, San Jose; **Sanjay Mehrotra**, Milpitas, all of Calif.

[73] Assignee: **SanDisk Corporation**, Sunnyvale, Calif.

[*] Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

This patent is subject to a terminal disclaimer.

[21] Appl. No.: **08/789,421**

[22] Filed: **Jan. 29, 1997**

Related U.S. Application Data

[63] Continuation of application No. 08/174,768, Dec. 29, 1993, Pat. No. 5,602,987, which is a continuation of application No. 07/963,838, Oct. 20, 1992, Pat. No. 5,297,148, which is a division of application No. 07/337,566, Apr. 13, 1989, abandoned.

[51] **Int. Cl.**[7] **G06F 11/00**

[52] **U.S. Cl.** **395/182.06**; 365/218; 395/182.05

[58] **Field of Search** 395/182.06, 430, 395/182.05; 365/218, 185.33, 185.18; 371/10.2

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[57] **ABSTRACT**

A system of Flash EEprom memory chips with controlling circuits serves as non-volatile memory such as that provided by magnetic disk drives. Improvements include selective multiple sector erase, in which any combinations of Flash sectors may be erased together. Selective sectors among the selected combination may also be de-selected during the erase operation. Another improvement is the ability to remap and replace defective cells with substitute cells. The remapping is performed automatically as soon as a defective cell is detected. When the number of defects in a Flash sector becomes large, the whole sector is remapped. Yet another improvement is the use of a write cache to reduce the number of writes to the Flash EEprom memory, thereby minimizing the stress to the device from undergoing too many write/erase cycling.

107 Claims, 5 Drawing Sheets